CLAIMS

What is claimed is:

1. A power estimation system, comprising:

a power parameter calculator that generates at least one switching power related parameter based on a first predetermined characterization and a first set of circuit design characteristics and generates at least one leakage power related parameter based on a second predetermined characterization and a second set of circuit design characteristics; and

a power estimator that determines switching power employing the at least one switching power related parameter and leakage power employing the at least one leakage power related parameter.

2. The system of claim 1, the at least one switching power related parameter comprising total switching capacitance and total crossover current.

3. The system of claim 2, the power estimator determines the switching power associated with the at least one unit of the circuit design by evaluating the equation:

$$P_{SWITCHING} = C_{SWITCHING} * V_{SUPPLY}{}^{2} * f + I_{CROSSOVER} * V_{SUPPLY}$$

where $C_{SWITCHING}$ is the total switching capacitance of the circuit design, V_{SUPPLY} is the supply voltage of the circuit design, f is the frequency of the clock of the circuit design, and $I_{CROSSOVER}$ is the total crossover current of the circuit design.

4. The system of claim 1, the first predetermined characterization comprising a predetermined activity factor list and the first set of circuit design characteristics comprising a node capacitance list associated with a circuit design instance, the power parameter calculator determines a total switching capacitance by multiplying node capacitance by a predetermined activity factor associated with a given node, and summing switching capacitances for a plurality of nodes of the circuit design.

5. The system of claim 4, the first predetermined characterization comprising a set of crossover current equations and the first set of circuit design

characteristics comprising respective device gate widths, input voltage slopes and capacitive load parameters associated with a channel connected region, the power parameter calculator determines crossover currents by evaluating respective crossover equations over a plurality of channel connected region of the circuit design, and summing the determined crossover currents.

6. The system of claim 1, the second predetermined characterization comprising at least one predetermined leakage coefficient and the second set of circuit design characteristics comprising transistor gate area, the power parameter calculator determines a total leakage current by multiplying total transistor gate area by the at least one predetermined leakage coefficient.

7. The system of claim 6, the power parameter calculator determines total gate tunneling leakage and total source-to-drain leakage of the at least one unit of the circuit design.

8. The system of claim 7, the power parameter calculator determines gate tunneling leakage by summing the transistor gate areas associated with p-type devices multiplied by a predetermined p-type coefficient and summing the transistor gate areas associated with n-type devices multiplied by a predetermined n-type coefficient.

9. The system of claim 7, the power parameter calculator determines source-to-drain leakage by summing the transistor gate areas associated with high voltage threshold (HVT)-type devices multiplied by a predetermined HVT-type coefficient and summing the transistor gate areas associated with low voltage threshold (LVT)-type devices multiplied by a predetermined LVT-type coefficient.

10. The system of claim 1, the at least one leakage power related parameter comprising total leakage current.

11. The system of claim 10, the power estimator determines the leakage power associated with the at least one unit of the circuit design by evaluating the equation:

$$P_{LEAKAGE} = I_{LEAKAGE} * V_{SUPPLY}$$

where $I_{LEAKAGE}$ is the total leakage current of the circuit design and V_{SUPPLY} is the supply voltage of the circuit design.

12. The system of claim 1, the first set of circuit design characteristics and the second set of circuit design instances are generated by an analysis tool for a plurality of circuit design instances, and first predetermined characterization and the second predetermined characterization are stored in memory prior to execution of the analysis tool.

13. A system for determining an estimation of power for a circuit design, the system comprising:

a switching capacitance calculator that determines switching node capacitance over a plurality of nodes by multiplying node capacitance by a predetermined activity factor associated with a given node over a plurality of nodes, and summing the determined switching capacitances to generate a total switching capacitance;

a crossover current calculator that determines crossover currents over a plurality of channel connected regions by evaluating predetermined crossover equations with respective crossover current parameters for a given channel connected region over a plurality of channel connected regions, and summing the determined crossover currents to generate a total crossover current;

a leakage current calculator that determines leakage currents for a plurality of transistor devices by multiplying predetermined leakage coefficients associated with a given transistor type by the sums of transistor gate areas associated with the given type for a plurality of transistor types, and summing the determined leakage currents to generate a total leakage current; and

a power estimator that employs the total switching capacitance, the total crossover current and the total leakage current to determine a total circuit power associated with the circuit design.

14. The system of claim 13, the power estimator determines the total circuit power associated with the circuit design by evaluating the equation:

$$P_{TOTAL} = C_{SWITCHING} * V_{SUPPLY}{}^{2} * f + I_{CROSSOVER} * V_{SUPPLY} + I_{LEAKAGE} * V_{SUPPLY}$$

where $C_{SWITCHING}$ is the total switching capacitance of the circuit design, V_{SUPPLY} is the supply voltage of the circuit design, f is the frequency of the clock of

the circuit design, $I_{CROSSOVER}$ is the total crossover current of the circuit design and $I_{LEAKAGE}$ is the total leakage current of the circuit design.

15. The system of claim 13, the node capacitance is provided by an analysis tool and the predetermined activity factor is provided from a predetermined activity factor list.

16. The system of claim 13, the crossover current calculator receives transistor device gate widths, input voltage slopes and capacitive load information associated with the channel connected regions from an analysis tool, and retrieves the predetermined crossover equations from a predetermined crossover equations list.

17. The system of claim 13, the leakage current calculator determines total gate tunneling leakage and total source-to-drain leakage of the circuit design, the gate tunneling leakage is determined by summing p-type transistor gate areas multiplied by a predetermined p-type coefficient and summing n-type transistor gate areas multiplied by a predetermined n-type coefficient, the source-to-drain leakage is determined by summing high voltage threshold (HVT)-type device areas multiplied by a predetermined HVT-type coefficient and summing low voltage threshold (LVT)-type area multiplied by a predetermined LVT-type coefficient.

18. A power estimation system, comprising:

means for determining switching power related parameters by evaluating predetermined characterizations that functionally relate a first set of circuit design characteristics as a function of switching power related parameters;

means for determining leakage power related parameters by evaluating predetermined characterizations that functionally relate a second set of circuit design characteristics as a function of leakage power related parameters; and

means for generating a total power estimate based on the switching power related parameters and the leakage power related parameters.

19. The system of claim 18, the means for determining switching power related parameters comprising means for determining crossover current and means for determining switching capacitance.

20. The system of claim 18, the means for determining leakage power related parameters comprising means for determining gate tunneling leakage and means for determining source-to-drain leakage.

21. A power estimation method for a circuit design, comprising:

computing at least one switching power related parameter based on a first set of circuit design characteristics and a first predetermined characterization of switching power related parameters as a function of the first set of circuit design characteristics;

computing at least one leakage power related parameter based on a second set of circuit design characteristics and a predetermined characterization of leakage power related parameters as a function of the second set of circuit design characteristics; and

determining total circuit design power based on the computed at least one switching power related parameter and the computed at least one leakage power related parameter.

22. The method of claim 21, the computing at least one switching power related parameter comprising determining switching capacitance by multiplying node capacitance by an associated predetermined activity factor for a plurality of nodes, and summing the switching capacitances to generate a total switching capacitance, and determining crossover current by evaluating predetermined equations that functional relate channel connected region characteristics to crossover current, and summing crossover current over a plurality of channel connected regions.

23. The method of claim 22, the computing at least one leakage power related parameter comprising determining gate tunneling leakage by adding a sum of transistor gate areas of p-type devices multiplied by a predetermined p-type leakage coefficient to a sum of transistor gate areas of n-type devices multiplied by a predetermined n-type leakage coefficient, and determining source-to-drain leakage by adding a sum of transistor gate areas of high voltage threshold (HVT)-type devices multiplied by a predetermined HVT-type leakage coefficient to a sum of transistor gate areas of low voltage threshold (LVT)-type devices multiplied by a predetermined LVT-type leakage coefficient.

24. A computer-readable medium having computer-executable instructions for performing the method of claim 23.

25. The method of claim 21, further comprising:

executing an analysis tool for a plurality of circuit design instances;

computing a plurality of power estimates associated with the plurality of circuit design instances; and

comparing the power estimates to determine an optimal circuit design.